Appl. No. 10/685,028
Amdt. dated August 4, 2006
Reply to Office action of May 5, 2006

Listing of Claims:

1. (Original) A system, comprising:

a timing logic unit coupled to produce a predetermined number of pulses in response to a transaction request transmitted from a source device to a target device, wherein the timing logic unit is configured to generate a time expired signal upon producing a last one of the predetermined number of pulses; and

a processor for executing program instructions configured to programmably alter a rate at which the predetermined number of pulses are produced by the timing logic unit, thereby adjusting an expiration period for completing a transaction cycle associated with the transaction request.

2. (Original) The system as recited in claim 1, wherein the program instructions are configured to programmably decrease the rate for increasing the expiration period.

3. (Original) The system as recited in claim 1, wherein the program instructions are configured to programmably increase the rate for decreasing the expiration period.

4. (Original) The system as recited in claim 1, wherein the timing logic unit is arranged within at least one of the source and target devices.

5. (Original) The system as recited in claim 4, further comprising a carrier medium configured to transfer information associated with the transaction cycle between the source device and the target device.

6. (Original) The system as recited in claim 5, wherein the carrier medium comprises one or more buses within a computer system, such that the source and target devices are each arranged within the computer system.

7. (Original) The system as recited in claim 5, wherein the carrier medium comprises a wired or wireless network interface for coupling the system to one or more additional systems, such that the source device is arranged within the system and the target device is arranged within one of the additional systems, or vice versa.

8. (Original) A computer system, comprising:

a source device configured to initiate a transaction cycle by sending a transaction request to a target device;

a timing logic unit arranged within the target device, wherein the timing logic unit comprises:

a time register for storing a predetermined expiration value;

a first counter for receiving a number of pulses corresponding to the predetermined expiration value, and generating a time expired signal upon receipt of a last one of the number of pulses; and

a memory device for storing program instructions configured to programmably alter a rate at which the number of pulses are received by the first counter, thereby adjusting an expiration period for completing the transaction cycle.

9. (Original) The computer system as recited in claim 8, wherein the program instructions are configured to programmably decrease the rate, thereby increasing the expiration period, if a target-ready signal is not asserted by the target device before the time expired signal is generated by the timing logic unit.

10. (Original) The computer system as recited in claim 8, wherein the program instructions are configured to programmably increase the rate, thereby decreasing the expiration period, if a target-ready signal and a source-ready signal are asserted by the target device and the source device, respectively, before the time expired signal is generated by the timing logic unit.

11. (Original) The computer system as recited in claim 9, wherein the target-ready signal is asserted upon completion of the transaction request by the target device, and wherein the source-ready signal is asserted when the source device is ready to send or receive transaction data, which corresponds to the transaction request, for completing the transaction cycle.

12. (Original) The computer system as recited in claim 10, wherein the target-ready signal is asserted upon completion of the transaction request by the target device, and wherein the source-ready signal is asserted when the source device is ready to send or receive transaction data, which corresponds to the transaction request, for completing the transaction cycle.

13. (Original) The computer system as recited in claim 8, further comprising a processor coupled for receiving interrupt signals from a clock source at a fixed rate and for executing the program instructions in response to the interrupt signals.

14. (Original) The computer system as recited in claim 13, wherein the timing logic unit further comprises:

a control register for storing an enable signal;

a second counter for generating the number of pulses; and

a circuit comprising the time register and the first counter, wherein the circuit is coupled to receive the enable signal and at least one of the number of pulses every n^{th} time the processor receives an interrupt signal, wherein 'n' is a programmable value selected from a group consisting of any positive, non-zero integer value.

15. (Original) The computer system as recited in claim 14, further comprising a primary bus bridge logic unit configured to coordinate transactions between the processor, the memory device, and one or more peripheral devices coupled to

the primary bus bridge logic unit over one or more peripheral buses of the computer system.

16. (Original) The computer system as recited in claim 15, wherein the timing logic unit is arranged within the primary bus bridge logic unit.

17. (Original) The computer system as recited in claim 15, wherein the timing logic unit is arranged within the one or more peripheral devices.

18. (Original) The computer system as recited in claim 15, further comprising a secondary bus bridge unit coupled to the primary bus bridge unit over one of the peripheral buses and having one or more additional peripheral devices coupled thereto, wherein the timing logic unit is arranged within the secondary bus bridge unit and/or within the one or more additional peripheral devices.

19.-36. (Canceled).